100 and 50 MHz Digital Waveform Generator/Analyzers

NI 654x

- 100 MHz maximum clock rate
- Compatible with 5.0, 3.3, 2.5, or 1.8 V logic (software-selectable)
- 32 channels with per-channel direction control
- 1, 8, or 64 Mb/channel onboard memory
- Interactive waveform and script editor software
- Synchronization and Memory Core (SMC) for tight synchronization with other SMC-based devices

Operating Systems

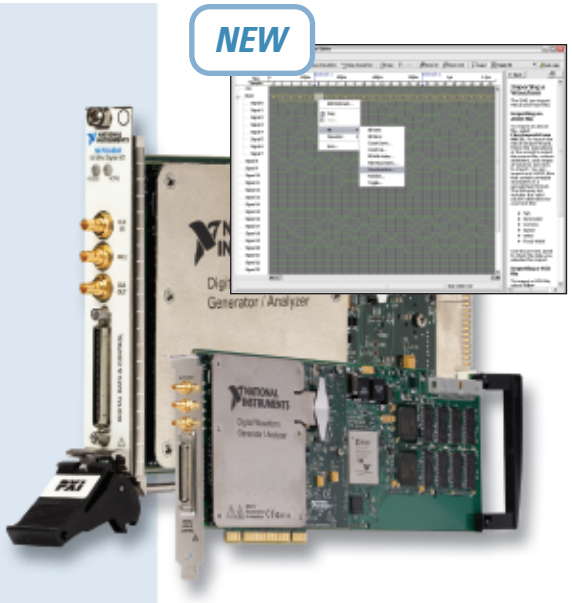
- Windows 2000/NT/XP

Recommended Software

- LabVIEW 7 Express or later
- LabWindows/CVI

Driver and Editing Software (included)

- NI-HSDIO
- LabVIEW 7.1 Express VIs
- Script Editor
- Digital Waveform Editor (included with 8 and 64 Mb/channel models only)



Product	Platform	Maximum Channels	Rate (MHz)	Compatible Logic Levels (V)	Memory (Mb/channel)	Scripting	Programmable Data Delay
NI 6542	PCI, PXI	32	100	5.0, 3.3, 2.5, or 1.8	1, 8, or 64	✓	✓
NI 6541	PCI, PXI	32	50	5.0, 3.3, 2.5, or 1.8	1, 8, or 64	✓	✓

Table 1. NI 654x Specifications Overview

Description

The National Instruments 6542 and 6541 devices are 100 and 50 MHz digital waveform generator/analyzers, respectively, for interfacing to digital electronics. These modules feature 32 channels with per-channel direction control and deep onboard memory with triggering and pattern sequencing. Through the NI-HSDIO driver, you can interface with 5.0, 3.3, 2.5, or 1.8 V logic. You can also use these devices with the NI Digital Waveform Editor, an interactive software tool for creating and editing digital waveforms. With the SMC, you can create mixed-signal test systems with digitizers, arbitrary waveform generators, and other digital waveform generator/analyzers, or you can synchronize multiple digital devices to build low-skew multichannel systems for interfacing to high pin count digital ICs and electronics.

Design High-Density Interfaces

- Data delay for clock frequencies ≥25 MHz
- Data delay resolution of 0.4% of clock period
- Internal or external sample or reference clock sources
- ±600 ps channel-channel skew (typ)
- ±32 mA maximum DC drive strength per channel (configured for 3.3 V logic)
- Multidevice synchronization with other SMC-based modular instruments

Applications
Semiconductor
Mixed-signal design validation and test
Interfacing to digital electronics
Aerospace/Defense
Subsystem emulation
Communications
Multimedia chipset emulation
Medical Electronics
Emulation of IC communications
Consumer Electronics
CMOS and CCD imaging sensors

Create and Edit Patterns Interactively with the Digital Waveform Editor

- Import existing waveforms into LabVIEW from VHDL simulation and spreadsheet tools in Value Change Dump (.VCD) or ASCII formats
- Create new waveforms using built-in fill patterns
- Edit waveforms interactively in the user interface
- Link and loop created digital waveforms with the Script Editor

Ordering Information

NI PCI-6541 .....778988-0M
NI PXI-6541 .....778952-0M[1]
NI PCI-6542 .....778989-0M
NI PXI-6542 .....778953-0M[1]

[1]Where M is: 1 (1Mb/channel), 2 (8 Mb/channel), or 3 (64 Mb/channel)
Includes NI-HSDIO driver and Script Editor. The 8 and 64 Mb/channel models also include the Digital Waveform Editor.

Software
NI Digital Waveform Editor 778724-03

Cable
SHC68-C68-D2 188142-01

Accessory
CB-2162 778592-01
SMB-2163 778747-01

BUY ONLINE!
Visit ni.com/info and enter pci6541, pci6542, pxi6541, pxi6542.

NATIONAL INSTRUMENTS™

100 and 50 MHz Digital Waveform Generator/Analyzers

Specifications

For detailed specifications, please visit ni.com/info and enter: pci6541, pci6542, pxi6541, pxi6542.
These specifications are valid for the following temperature ranges: PCI: 0 to 45 °C, PXI: 0 to 55 °C.

Channel Characteristics

Number of data channels 32
Direction control of data channels ..... Per channel

Generation Signal Characteristics (data, DDC ClkOut, and PFI <0:3> channels)

All voltage ranges specified into 1 MΩ
Generation voltage families (V) ..... 1.8, 2.5, 3.3 logic families (5 V compatible)
Generation signal type ..... Single-ended

Generation voltage levels

Family	Low Voltage Levels (V)		High Voltage Levels (V)		I=100 µA
Settings (V)	Typical	Max	Min	Typical	
1.8	0	0.1	1.7	1.8	
2.5	0	0.1	2.4	2.5	
3.3	0	0.1	3.2	3.3	
5.0	0	0.1	3.2	3.3	

Output impedance ..... 50 Ω nominal at 25 °C
Maximum DC drive strength ..... ±8 mA at 1.8 V
±16 mA at 2.5 V
±32 mA at 3.3 V
Channel power-up state ..... Drivers disabled, 10 kΩ input impedance

Acquisition Signal Characteristics (data, strobe, and PFI <0:3> channels)

Acquisition voltage families (V) ..... 1.8, 2.5, 3.3, 5.0 logic families

Acquisition voltage levels

Family	Low Voltage Thresholds (V)	High Voltage Thresholds (V)
Settings (V)	Max	Min
1.8	0.45	1.35
2.5	0.75	1.75
3.3	1.0	2.3
5.0	1.0	2.3

Input impedance ..... High impedance (10 kΩ)

Timing Characteristics

Sample Clock

Sample clock sources ..... 1. Onboard clock (internal VCXO with divider)
2. CLK IN (SMB)
3. PXI_STAR (PXI only)
4. STROBE (DDC Connector) – Acquisition only
On board clock frequency range ..... NI 6541: 48 Hz to 50 MHz.
(Settable to 200 MHz / N; 4 ≤ N ≤ 4,194,304)
NI 6542: 48 Hz to 100 MHz.
(Settable to 200 MHz / N; 2 ≤ N ≤ 4,194,304)
Exported sample clock delay range ..... 0 - 1 sample clock periods for clock frequencies ≥ 25 MHz
Exported sample clock delay resolution ..... 1/256 of sample clock period for clock frequencies ≥ 25 MHz

Exported sample clock jitter (typical using onboard clock)

Period jitter	Cycle-to-cycle jitter
20 ps (rms)	35 ps (rms)

Generation Signal Characteristics (data, DDC Clk Out, and PFI <0:3> channels)

Data channel-to-channel skew ..... ±600 ps (typical across all data channels)
Maximum data channel toggle rate ..... NI 6541: 25 MHz; NI 6542: 50 MHz
Data position modes ..... Rising edge, falling edge, delayed relative to sample clock
Generation data delay range ..... 0 - 1 sample clock period for clock frequencies ≥ 25 MHz
Generation data delay resolution ..... 1/256 of sample clock period for clock frequencies ≥ 25 MHz

Acquisition Signal Characteristics (data, strobe, and PFI <0:3> channels)

Channel-to-channel skew ..... ±600 ps (typical across all data channels)
Acquisition timing delay range ..... 0 - 1 sample clock periods for clock frequencies ≥ 25 MHz
Acquisition timing delay resolution ..... 1/256 of sample clock period for clock frequencies ≥ 25 MHz

Waveform Characteristics

Memory and Scripting

Onboard memory size (assumes no scripting instructions)	1 Mb/channel (for generation sessions)	8 Mb/channel (for generation sessions)	64 Mb/channel (for generation sessions)
	1 Mb/channel (for acquisition sessions)	8 Mb/channel (for acquisition sessions)	64 Mb/channel (for acquisition sessions)

Generation modes

Waveform: Generate a single waveform once, N times, or continuously.
Scripted: Generate a simple or complex sequence of waveforms. Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to script triggers.

Triggers (inputs to the NI 654x)

Trigger types ..... Start Trigger, Pause Trigger, Script Trigger <0:3> (Generation sessions only), Reference Trigger (Acquisition sessions only)
Sources ..... 1. PFI <0> (SMB Jack connectors)
2. PFI <1:3> (DDC connector)
3. PXI_TRIG<0:7> (PXI backplane, PXI only)
RTSI <0..7> (PCI only)
4. PXI STAR (PXI backplane, PXI only)
5. Pattern match (Acquisition sessions only)
6. Software (User function call)
7. Disabled (Do not wait for a trigger)
Trigger detection ..... 1. Start Trigger (Edge detection: rising or falling)
2. Pause Trigger (Level detection: high or low)
3. Script Trigger <0:3> (Edge detection: rising or falling, Level detection: high or low)
4. Reference Triggers (Edge detection: rising or falling)
Minimum required trigger pulse width ..... 40 ns
Destinations ..... 1. PFI <0> (SMB Jack Connector)
2. PFI <1:3> (DDC Connector)
3. PXI_TRIG <0:7> (PXI Backplane)
RTSI <0..7> (PCI only)
Each of the Triggers can be routed to any of the 13 Destinations with the exception of Pause Trigger. Pause Trigger can not be exported.

Events (outputs from the NI 654x)

Event types ..... Marker <0..3>, Data Active Event, Ready for Start Event
Destinations ..... 1. PFI <0> (SMB Jack Connectors)
2. PFI <1:3> (DDC Connector)
3. PXI_TRIG <0:7> (PXI Backplane)
Each of the Events can be routed to any of the destinations with the exception of Data Active Event. Data Active Event can only be routed to the PFI channels.

Miscellaneous

Onboard Clock characteristics (Only valid when PLL Reference Source is set to None)

Frequency accuracy ..... ±100 ppm (typical)
Temperature stability ..... ±30 ppm (typical)
Aging ..... ±5 ppm first year (typical)

Power Requirements

Typical ..... 15 W
Maximum ..... 20.5 W

Physical

Dimensions
PCI ..... 12.6 cm by 35.5 cm (4.95 in. by 13.9 in.)
PXI ..... Single 3U CompactPCI Slot. PXI Compatible

I/O Panel Connectors

Label	External Function(s)	Connector Type
CLK IN	Sample Clock, External PLL Reference Input	SMB jack
PFI 0	Events, Triggers	SMB jack
CLK OUT	Exported Sample Clock, Exported Reference Clock	SMB jack
Digital data and Control (DDC)	Digital data channels, Exported Sample Clock, STROBE, Events, Triggers	68 pin VHDCI

Environment

Operating temperature ..... PCI: 0 to 45 °C
PXI: 0 to 55 °C in all NI PXI chassis except the following. 0 to 45 °C when installed in an NI PXI-1000/B and PXI-101x chassis. (Meets IEC-60068-2-1 and IEC-60068-2-2)
Storage temperature ..... -20 to 70 °C
Relative humidity ..... 10 to 90% relative humidity, noncondensing (meets IEC-60068-2-56)
Storage Relative humidity ..... 5 to 95% relative humidity, noncondensing (meets IEC-60068-2-56)

Compliance

Safety
NI 654x devices meet the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:
IEC 61010-1, EN 61010-1
UL 3111-1, UL 61010B-1
CAN/CSA C22.2 No. 1010.1
Note: For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. See the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit ***ni.com/hardref.nsf***

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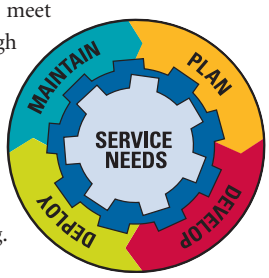

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